ABSTRACT

[0048] The present invention is a method circuit and system for erasing one or more non-volatile memory ("NVM") cells in an NVM array. One or more NVM cells of a memory array may be erased using an erase pulse produced by a controller and/or erase pulse source adapted to induce and/or invoke a substantially stable channel current in the one or more NVM cells during an erasure procedure. The voltage profile of an erase pulse may be predefined or the voltage profile of the erase pulse may be dynamically adjusted based on feedback from a current sensor during an erase procedure